Electronic Version
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Claims

[c1] 1. A semiconductor structure formed on a substrate comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

an inverter receiving said ring oscillator output as an input, said inverter being coupled to a device under test and said inverter receiving a third voltage and a fourth voltage as power supplies,

wherein current drawn by said inverter provides a measurement of capacitance of said device under test.

[c2] 2. The structure in claim 1, wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

[c3] 3. The structure in claim 1, wherein a difference between said third and fourth is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

[c4] 4. The structure in claim 1, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure.

[c5] 5. The structure in claim 4, wherein said capacitance constant is for said semiconductor structure alone and does not include any part of said capacitance of said device under test.

[c6] 6. The structure in claim 1, wherein said measurement of capacitance of said device under test is used to determine the thickness of a gate oxide.

[c7] 7. The structure in claim 1, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

[c8] 8. An on-chip test device comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

an inverter receiving said ring oscillator output as an input, said inverter being coupled to a device under

test and said inverter receiving a third voltage and a fourth voltage as power supplies,

wherein said on-chip test device and said device under test are located on the same semiconductor chip; and

wherein current drawn by said inverter provides a measurement of capacitance of said device under test.

[c9] 9. The device in claim 8, wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

[c10] 10.The device in claim 8, wherein a difference between said third and fourth voltages is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

[c11] 11.The device in claim 8, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure

[c12] 12.The device in claim 11, wherein said capacitance constant is for said on-chip test device alone and does not include any part of said capacitance of said device under test.

[c13] 13.The device in claim 8, wherein said measurement of capacitance of said device under test is used to determine the thickness of a gate oxide.

[c14] 14.The device in claim 8, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

[c15] 15.A semiconductor structure formed on a substrate comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

a plurality of inverters receiving said ring oscillator output as an input, each inverter being coupled to a different terminal of a multi-terminal device under test, wherein said inverters receive a third voltage and a fourth voltage as power supplies,

wherein current drawn a first inverter of said inverters provides a measurement of capacitance of a first terminal of said multi-terminal device under test while remaining ones of said inverters isolate current

drawn by said first inverter to only that associated with said first terminal.

[c16] 16.The structure in claim 15, wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

[c17] 17.The structure in claim 15, wherein a difference between said third and fourth is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

[c18] 18.The structure in claim 15, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure.

[c19] 19.The structure in claim 18, wherein said capacitance constant is for said semiconductor structure alone and does not include any part of said capacitance of said device under test.

[c20] 20.The structure in claim 15, wherein said measurement of capacitance of said device under test is used to deter-

mine the thickness of a gate oxide.

[c21] 21.The structure in claim 15, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

[c22] 22.A method of testing the capacitance of a device under test in an integrated circuit chip, said method comprising:

supplying an output of a ring oscillator to an inverter to produce an inverted ring oscillator output, wherein said inverter receives different voltages as power supplies; and

inputting said inverted ring oscillator output to said device under test,

determining current drawn by said inverter to provide a measurement of capacitance of said device under test.

[c23] 23.The method in claim 22, wherein said difference between said voltages is less than or equal to approximately one-third of the difference between a second set of voltages provided to said ring oscillator.

[c24] 24.The method in claim 22, wherein said difference between said voltages is less than the sum of absolute values of threshold voltages of n-type and p-type field ef-

fect transistors that comprise said inverter.

[c25] 25.The method in claim 22, further comprising calculating said capacitance by:

multiplying the frequency of said ring oscillator output by the difference between said voltages to produce a first result;

dividing said current drawn by said inverter by said first result to produce a second result; and

subtracting a capacitance constant for a testing device from said second result.

[c26] 26.The method in claim 22, wherein said capacitance constant is for said testing device alone and does not include any part of said capacitance of said device under test.

[c27] 27.The method in claim 22, wherein said device under test comprises a gate oxide capacitor.

[c28] 28.The method in claim 27, wherein said measurement of capacitance of said device under test is used to determine the thickness of said gate oxide capacitor.

[c29] 29.The method in claim 22, wherein said device under test comprises one of a gate conductor, a channel, and an interconnect.